

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6	"6366878".pn. "5357626".pn. "4176258".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 16:20
L2	0	1 and fpga	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 15:43
L3	1	1 and trace	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 16:24
L4	0	1 and sram	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 16:24
S6	2	profit.in. and emulator	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 16:02
S22	0	"ep 1 205 848 A1"	EPO	OR	OFF	2006/08/03 16:02
S23	0	"ep1205848A1"	EPO	OR	OFF	2006/08/03 16:03
S24	1	"1205848"	EPO	OR	OFF	2006/08/03 17:11
S25	0	(cache same compar\$5) and (lock\$step)	EPO	OR	OFF	2006/08/03 17:12
S26	236	(cache same compar\$5) and (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:12
S27	0	S26 and (714/28.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:13
S28	0	S26 and (714/29.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:13

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S29	1	S26 and (714/30.ccls.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:19
S30	1	S26 and ("703".clas.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:19
S31	0	S26 and "716".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:20
S32	75	S26 and "714".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:22
S33	2	S32 and (ICE (in\$circuit\$emulat\$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:27
S34	2	"4,176,258".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/03 17:27
S35	48	("3636443" "3815025" "3913072" "4038648").PN. OR ("4176258").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/08/04 10:48
S36	0	S35 and microcontroller	US-PGPUB; USPAT; USOCR	OR	OFF	2006/08/04 10:48
S37	100	714/30.ccls. and microcontroller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/04 10:49
S38	0	S37 and lock\$step	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/04 10:49

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S39	64	microcontroller and ((cache register memory) same compar\$5) and (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/08/04 10:50
S40	123	microcontroller and ((cache register memory) same compar\$5) and (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/04 10:54
S41	13	S40 and "714".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/04 10:52
S42	3	S40 and "703".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/04 10:53
S43	1	S40 and "717".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/04 10:53
S44	107	S40 not (S41 S42 S43)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 13:58
S45	4203	((parallel lock\$step) same microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 13:59
S46	42	S45 and "703".clas.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 13:59
S47	6	((lock\$step) same microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:00
S48	575	(debug\$4 same microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:02

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S49	6	S48 and (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:01
S52	247	S48 and (compar\$5 same (memory register contents))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:03
S53	199	S48 and (compar\$5 with (memory register contents))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:03
S54	2	(lock\$step same microcontroller same (compar\$5 detect\$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:04
S55	6	(lock\$step same microcontroller and (compar\$5 detect\$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:05
S56	20	(lock\$step same embedded and (compar\$5 detect\$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:06
S57	78	(lock\$step and microcontroller and emulat\$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:06
S58	78	S57 and (compar\$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:12
S59	785	(master and slave) same (microcontroller)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:13
S60	0	((master and slave) same (microcontroller)) same (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:13

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S61	4	((master and slave) same (microcontroller)) and (lock\$step)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 14:15
S62	19	((master and slave) same (microcontroller)) same (compar\$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/08/05 15:43